REMARKS

Applicant respectfully requests re-consideration of the application in view of the arguments presented below.

Summary of Office Action

Claims 1-16 are pending.

The title was objected to.

Claim 1 was rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,023,754 of DuLac, et al. ("DuLac").

Claim 2 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of U.S. Patent Publication No. 2004/0266065 of Zhang, et al. ("Zhang")

Claims 3, 5 were rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of U.S. Patent No. 6,102,710 of Beilen, et al. ("Beilin").

Claim 4 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of U.S. Patent Publication No. 2004/0059970 of Wieberdink, et al. ("Wieberdink").

Claim 6 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of U.S. Patent Publication No. 2003/0021232 of Duplaix, et al. ("Duplaix").

Claims 7-11 were rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of U.S. Patent No. 6,752,665 of Kha, et al. ("Kha").

Claim 12 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Kha and Zhang.

Claims 13 and 15 were rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Kha and Beilin.

Claim 14 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Kha and Wieberdink.

Claim 16 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Kha and Duplaix.

Summary of Amendments

The title was amended. Applicant submits that the amendment to the title does not add new matter.

Response to objection to title

Applicant has amended the title. Applicant respectfully submits that the Examiner's objection to the title is overcome.

Response to 35 U.S.C. § 102 rejections

Claim 1 was rejected under 35 U.S.C. § 102 as being anticipated by DuLac. Applicant notes: "A claim is anticipated *only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.*" Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)(*emphasis added*). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant submits that claim 1 is not anticipated by DuLac. In particular, *DuLac does not teach or disclose (1) controller circuit boards, (2) a storage array circuit board, and (3) a signal routing circuit board having connectors to couple the storage array circuit board and the input/output controller board.*

DuLac includes a disclosure of a bus switch for bus mapping between a host and a disk array. The bus switch selectively couples a plurality of controller busses to a plurality of drive busses. (DuLac, col. 3, lines 25-54)

Even if we assumed *arguendo* that DuLac included a disclosure of the various *circuits* (I/O controller circuit, storage array circuit, and signal routing circuit) alleged by the Examiner, there is no teaching or suggestion within DuLac as to the distribution of those circuits *across different boards*. Indeed, the term "board" was conspicuously missing from the Examiner's analysis. (see, 08/24/2005 Office Action, p. 3). Applicant further submits that the Examiner's references to Figure 2 of DuLac did not identify connectors for connecting boards to each other.

At best, Figure 2 of DuLac illustrates a plurality of modules and electrical paths between those modules. There is no teaching or suggestion of whether the modules are distributed across more than one circuit board nor of any connectors for connecting the modules or boards in such a case.

Thus applicant respectfully submits *DuLac does not teach or suggest (1) input/output controller boards, (2) storage array circuit board, and (3) a signal routing circuit board having connectors to couple to the storage array circuit board and the input/output controller board.*

In contrast, claim 1 includes the language:

> 1. An apparatus comprising:
> *input/output (I/O) controller circuit boards;*
> *a storage array circuit board* having storage device connectors to couple storage devices to the storage array circuit board; and
> *a signal routing circuit board having one or more connectors to couple the storage array circuit board to the signal routing circuit board, connectors to couple I/O controller circuit boards to the signal routing circuit board,* and one or more multiplexers to route data signals in a selective manner along one or more first data signal paths between a first I/O controller circuit board and the storage array circuit board and along one or more second data signal paths between a second I/O controller circuit board and the storage array circuit board, wherein the second data signal path(s) share a portion of one or more data signal paths of the first data signal path(s).

(Claim 1)(*emphasis added*)

Applicant thus submits claim 1 is not anticipated by DuLac. Applicant submits that the 35 U.S.C. § 102 rejections have been overcome.

Response to 35 U.S.C. § 103 rejections

Claims 2-16 were rejected as being unpatentable over DuLac in view of various combinations of Zhang, Beilen, Wieberdink, Duplaix, and Kha.

With respect to claims 2-6, applicant submits that none of Zhang, Beilen, Wieberdink, Duplaix, or Kha makes up for the deficiencies of DuLac as set forth in the response to the 35 U.S.C. § 102 rejections argued above. Accordingly, claim 1 is patentable over the cited references. Given that claims 2-6 depend from claim 1, claims 2-6 are likewise patentable over the cited references.

With respect to claims 7-16, applicant submits that the arguments presented above for the 35 U.S.C. § 102 arguments similarly apply. None of the cited references, alone or combined, teaches or suggests a particular distribution of the functionality across different circuit boards. In particular, DuLac *does not teach or suggest (1) an input/output controller board, (2) storage array circuit board, and (3) a signal routing circuit board removably connectable to the storage array circuit board and the input/output controller board.*

In contrast, claim 7 includes the language:

> 7. A storage system comprising:
> a housing;
> *a storage array circuit board* for mounting in the housing, the storage array circuit board having a plurality of storage device connectors for removably coupling a plurality of storage devices to the storage array circuit board;
> *at least one input/output (I/O) controller circuit board* for insertion in the housing, each I/O controller circuit board for communicating with storage devices; and
> *a signal routing circuit board* having electronics common to circuit boards connected thereto, *the signal routing circuit board for removable connection to the storage array circuit board and with each I/O controller circuit board,*
> wherein the electronics are removable from the housing without removal of the storage array circuit board.

(Claim 7)(*emphasis added*)

Applicant thus submits claim 7 is patentable under 35 U.S.C. § 103 over the cited references.

Given that claims 8-16 depend from claim 7, applicant submits claims 8-16 are likewise patentable over the cited references.

Applicant submits that the rejections under 35 U.S.C. § 103 have been overcome.

Conclusion

In view of the amendments and arguments presented above, applicant respectfully submits the applicable rejections and objections have been overcome. Accordingly, claims 1-16 should be found to be in condition for allowance.

If there are any issues that can be resolved by telephone conference, the Examiner is respectfully requested to contact the undersigned at **(512) 858-9910.**

Respectfully submitted,

Date November 4, 2005 William D. Davis

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